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(54) Image storage and retrieval

(57) Electronic document image storage and retrieval system having at least one image storage unit and a plurality of image display terminals. Under the control of a system controller, information in the storage unit can be supplied to a requesting terminal. The system controller includes a main printed circuit (PC) board 51 which has first and second generally parallel sets of busses 52, 53. The first set is separated electrically into at least first and second bus sections 52*a*, 52*b* (or 52*c*). The second set is electrically separated into at least first, second and third bus sections 53*a*, 53*b*, 53*c*. A plurality of host PC boards 56 and at least one direct memory access (DMA) image storage unit controller PC board 68 or 69 are provided. The host and DMA boards are mounted on the main board and are connected to the bus section 52*a*. The host boards are connected to the bus section 53*a* and the DMA board is connected to the bus section 53*b* or 53*c*. A plurality of memory PC boards 73 are mounted on the main board and are connected to the bus section 52*b* (or 52*c*). The section of the second set of busses 53 connected to the DMA board is connected (77, 78) to the section of the first of busses 52 connected to the memory boards.

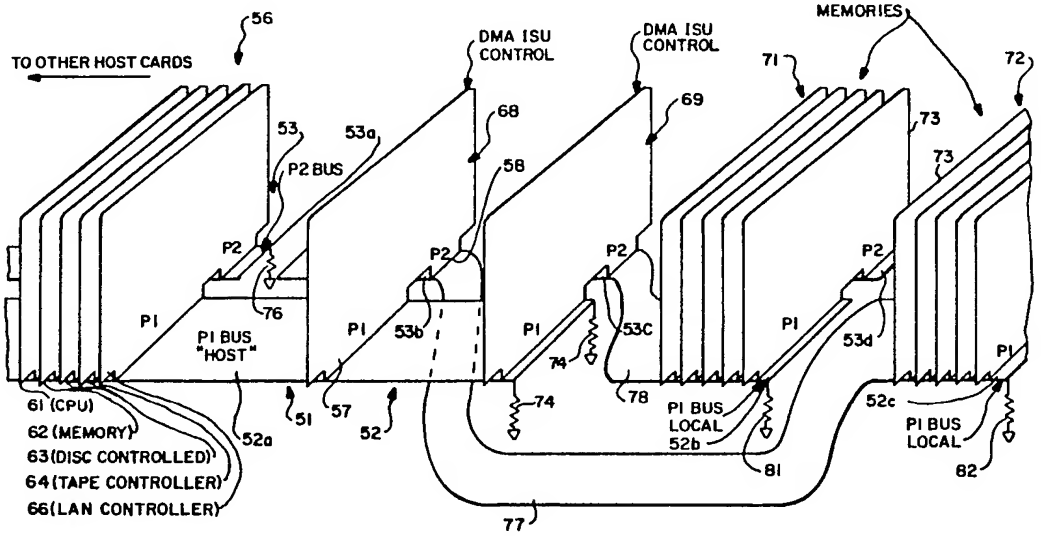

FIG.—2

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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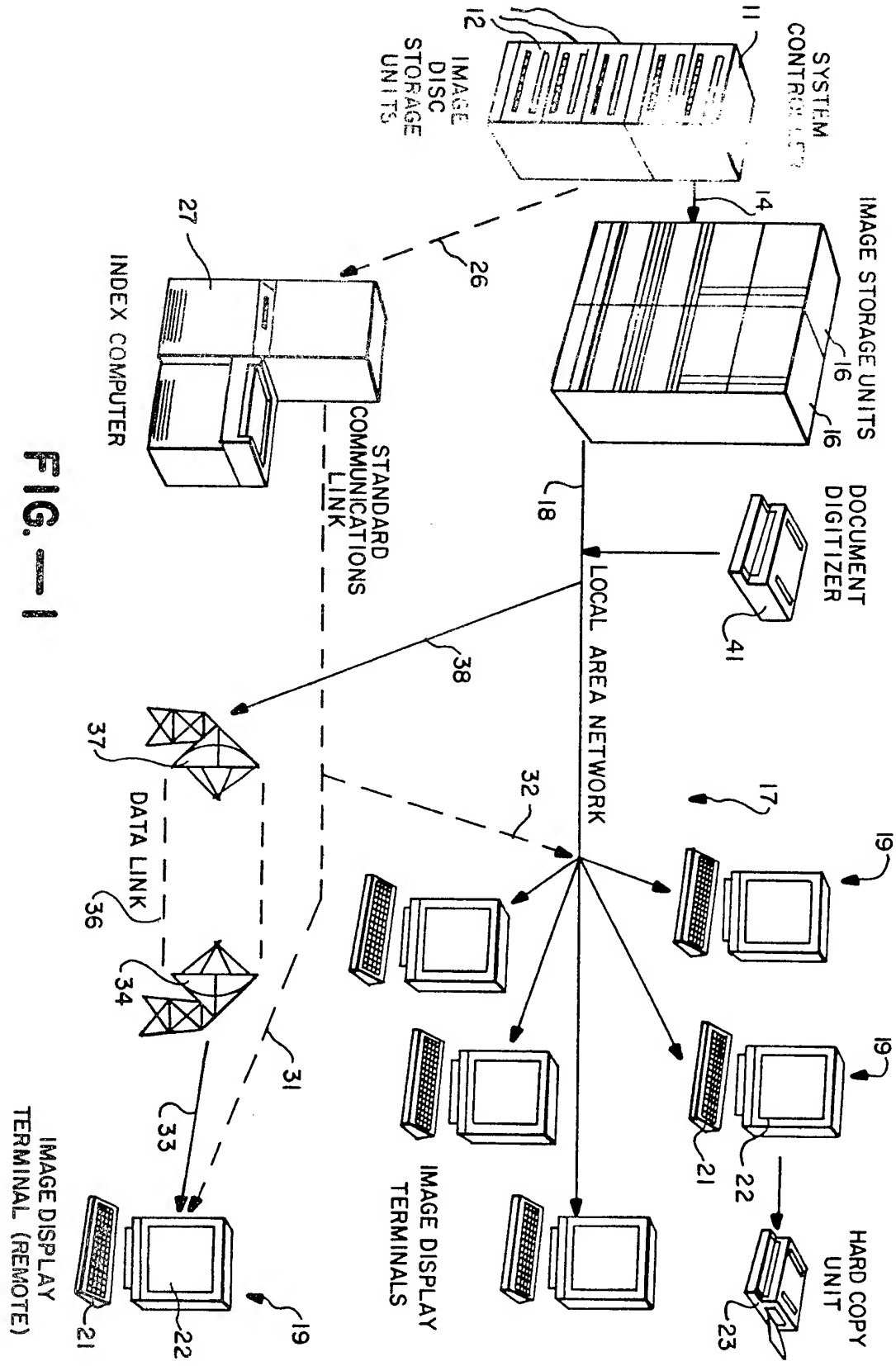
SYSTEM CONTROLLER
11
12
IMAGE DISC STORAGE UNITS
14
IMAGE STORAGE UNITS
16
16
18
26
27
INDEX COMPUTER
STANDARD COMMUNICATIONS LINK
DOCUMENT DIGITIZER
41
LOCAL AREA NETWORK
38
37
DATA LINK
36
32
34
31
33
17
19
19
21
22
IMAGE DISPLAY TERMINALS
HARD COPY UNIT
23
IMAGE DISPLAY TERMINAL (REMOTE)
21
22
19

FIG. — 1

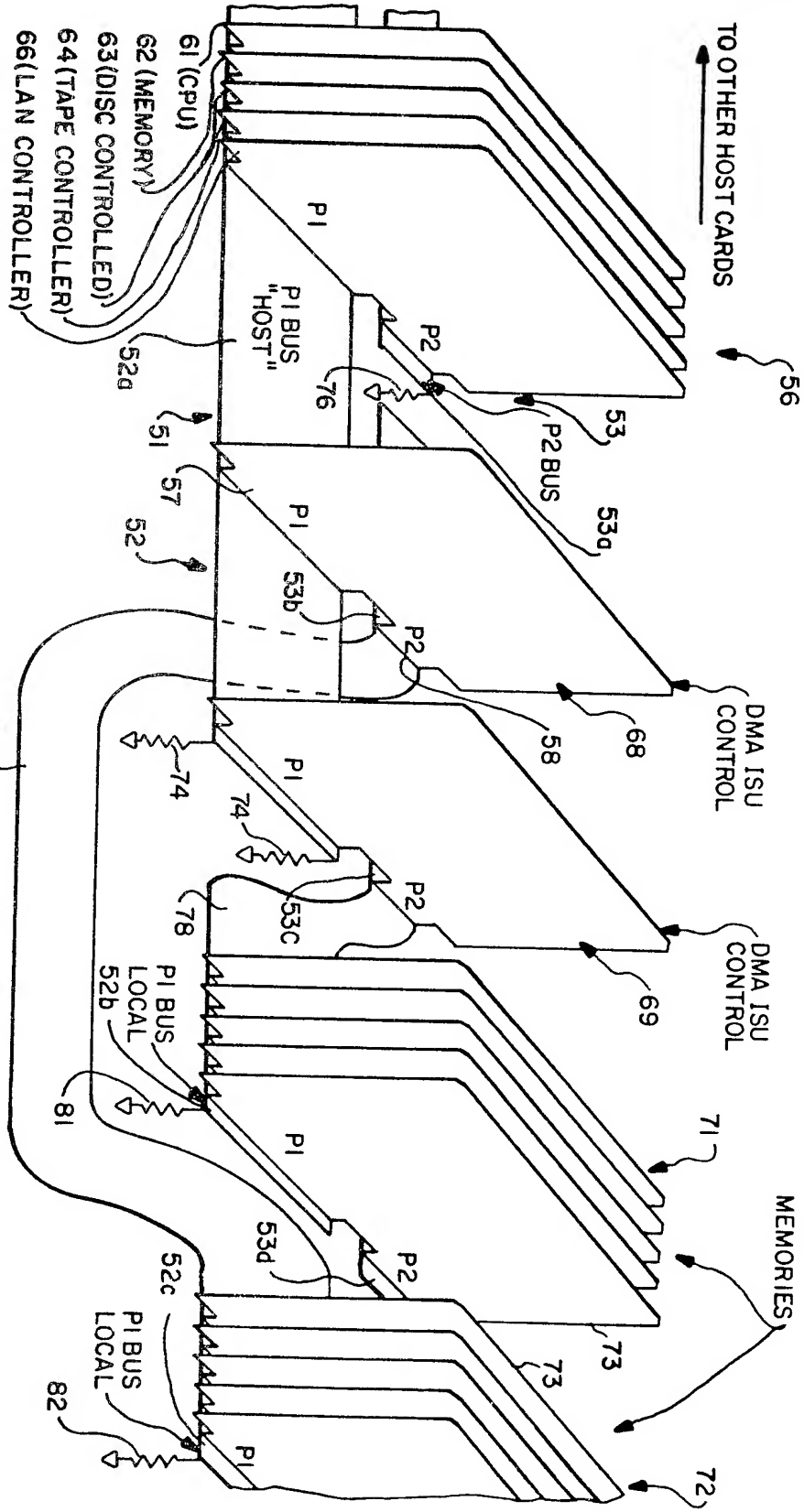
TO OTHER HOST CARDS
56
61 (CPU)
62 (MEMORY)
63 (DISC CONTROLLED)
64 (TAPE CONTROLLER)
66 (LAN CONTROLLER)
P1
P2
P1 BUS "HOST"
52a
76
53
P2 BUS
53a
51
57
52
53b
58
68
DMA ISU CONTROL
77
74
74
53c
78
69
DMA ISU CONTROL
P1 BUS LOCAL 52b
81
71
MEMORIES
53d
52c
73
73
P1 BUS LOCAL
82
72

FIG. 2

SPECIFICATION

Electronic document image storage and retrieval apparatus and system using a direct memory access controller

This invention relates to an electronic document image storage and retrieval apparatus and system and more particularly to one of this type utilizing a direct memory access controller.

Electronic document image storage and retrieval apparatus and systems have heretofore been provided. However, at the present time there is a necessity to interface with an image storage unit of the type described in co-pending application Serial No. 687,206 filed 12/28/1984 (A 40267) which produces a serial bit stream. Each time the image storage unit receives a request for scan of an image on the fiche of the roll film storage, the image storage unit sends a half megabyte of data which cannot be slowed or throttled. Thus there is a necessity to handle roughly a megabyte of serial information in approximately two seconds. If a standard bus is utilized for transferring this information, this bus typically has a limited bandwidth which determines the quantity of data which can be moved over the bus within a predetermined period of time. In addition, it is desirable not to utilize the full capacity of the bus so that bandwidth will be available whereby additional operations can be performed at the same time that information is being received from the image storage unit. Therefore there is a need for a system and apparatus of this type which is provided with a direct memory access controller.

In general, it is an object of this invention to provide an electronic document image storage and retrieval apparatus and system which utilizes a direct memory access controller.

Another object of the invention is to provide an apparatus and system of the above character which is fully automated by computer control and which provides on-line record storage and retrieval with fast access and excellent image quality.

Another object of the invention is to provide an apparatus and system of the above character in which data can be transferred from an image storage unit into a local memory.

Another object of the invention is to provide an apparatus and system of the above character in which multiple busses are utilized for the transfer of information.

Another object of the invention is to provide an apparatus and system of the above character in which the multiple busses have a sufficient capacity so that information can be moved into or out of memory one or more image storage units while at the same time reserving capacity for performing other operations during the same time that information is being transferred.

Another object of the invention is to provide an apparatus and system of the above character in which data can be transferred at a fast rate over the multiple busses and which at the same time provides reserve capacity on the multiple bus so that the controller and the memory can be accessed.

Another object of the invention is to provide an apparatus and system of the above character which is modular and can be readily expanded.

Another object of the invention is to provide an apparatus and system of the above character which provides high capacity image storage.

Another object of the invention is to provide an apparatus and system of the above character in which multiple image storage units can be utilized which operate under computer control.

Another object of the invention is to provide an apparatus and system of the above character which can utilize an image storage unit having the image information stored in roll form.

Another object of the invention is to provide an apparatus and system of the above character which can be constructed from Multibus components which have been modified to provide electrically isolated bus sections making possible the use of resident local memories.

Another object of the invention is to provide an apparatus and method of the above character in which an address extension register is provided.

Additional objects and features of the invention will appear from the following description in which preferred embodiments are set forth in detail in conjunction with the accompanying drawing.

Figure 1 is a block diagram of an electronic image storage and retrieval system incorporating the present invention.

Figure 2 is a schematic isometric view illustrating the multiple busses which have been utilized to provide direct memory access.

The electronic document image storage and retrieval system consists of at least one image storage unit and a plurality of image display terminals. Each image display terminal includes a video monitor and a keyboard. Each image display unit is adapted to be coupled to the image storage unit. A system controller is coupled to the image storage unit for controlling the operation of the image storage unit, whereby information carried in the image storage unit can be supplied to an image display terminal upon receipt of a request from the image display terminal. The system controller includes a main bus printed circuit board lying in a single plane. First and second generally parallel sets of busses are provided extending in one direction on the main printed circuit board. The first set of busses is separated electrically into at least first and second bus

sections. The second set of busses is electrically separated into at least first, second and third bus sections. A plurality of host printed circuit boards and at least one direct memory access image storage unit controller printed circuit board are provided. Means is provided for mounting said host printed circuit boards and said at least one direct memory access image storage unit controller printed circuit board on said main printed circuit board so that they extend at an angle therefrom and are electrically connected to the first section of the first set of busses and so that the host printed circuit boards are electrically connected to the first section of the second set of busses and the direct memory access image storage unit controller card is connected to the second section of the second set of busses. A plurality of memory printed circuit boards are provided. Means is provided for mounting said memory printed circuit boards on the main printed circuit board so that they extend at an angle therefrom and are electrically connected to the second section of the first set of busses. Means is provided for electrically connecting the second section of the second set of busses connected to the direct memory access image storage unit controller printed circuit board to the second section of the first set of busses.

The electronic document image storage and retrieval apparatus system shown in Figure 1 incorporating the present invention consists of a system controller 11 which includes direct memory access capability. The system controller can be of a conventional type and is based upon a single central processing unit based upon a Motorola (RTM) 68000 CPU. Additional details of the system controller 11 are hereinafter described. A plurality of image disc storage units 12 to provide a buffer storage are mounted in the same cabinet with the system controller 11. The image disc storage units can be of a conventional type, for example, it can be of a conventional Winchester drive with three discs and providing approximately 169 megabytes of memory per unit.

The system controller 11 is connected by a communication link 14 to image storage units 16. The image storage units 16 are of a type described in co-pending application serial number 687,206 filed 12/28/1984 (A 40267). Each of the image storage units 16 includes two separate film transport with each transport carrying a roll of microfilm having fiche thereon. As many as one million images can be stored in fiche on one roll of film. The image storage unit 16 also includes a built-in micro computer and a charge coupled array device to scan reduced microfilm images in the fiche electronically to produce for each image a 4 million binary bit stream. The bit stream can be handled as computer data.

The systems controller 11 is connected to a local area network (LAN) composed of a suitable means such as a coaxial cable 18 which carries the bit streams for conversion back to full size document display and hard copy. The local area network 17 is comprised of a plurality of remote locations, all of which have image display terminals 19 having dual mode capabilities. Each image display terminal includes a keyboard 21 and a high resolution screen 22. If desired, hard copy units 23 can be provided at the remote locations to provide hard copies when desired. They have the capability of receiving the bit streams and converting them to a full size printed document.

Each data display terminal 19 is provided with two connections from a data transfer point of view. On the one hand, each image display terminal is an intelligent device and is based upon a Motorola (RTM) 68000 microprocessor. Thus it is attached to the local area network via a local area network controller controlled by the Motorola (RTM) 68000 microprocessor. The other connection is from a data transfer point of view is via a standard RS 232 data communications cable 26 which is connected to an index computer 27. Thus, for example, if an operator at an image display terminal 19 wishes to select a particular document, the document desired is ascertained by the use of the index computer 27. The index computer 27 is utilized for selecting the proper document. Each document when it is being microfilmed is given a unique identification so it can be selected easily and referred to for display or copying. After the identification for a document has been determined, the operator utilizes the appropriate image display terminal 19 to send a request to the index computer 27 which in turn causes a command to be sent to the image display terminal 27 and automatically transferred to the system controller 11 which causes operation of the appropriate image storage unit 16 to send the image of the fiche over the coaxial cable 18 to the image display terminal 19.

Thus it can be seen that the image display terminal serves two major functions and operates in two modes. It serves as an interface to the index computer 27 as well as being the interface with the system controller 11. When the operator at the image display terminal 19 desires a hard copy, it is merely necessary to ascertain that the appropriate document is displayed on the screen of the display terminal and then causing the copy unit to provide a hard copy of the displayed image. Typically the hard copy unit 23 can have the same resolution as the screen, as for example, 200 dots per inch in both horizontal and vertical directions. As can be seen, the hard copy unit 23 is not connected into the local area network and for that reason the desired image must first be displayed on the screen and then the information supplied to the hard copy unit 23 through the image display terminal 19.

It should be appreciated that if desired, the index computer 27 can be in the same location as the system controller 11 and the image storage units 16. However, in large systems for large organizations, it may be desirable to have a central index computer 27 accessible to a number of system controllers 11 and image storage units 16 located at different locations. Thus the index computer 27 can be connected to system controllers 11 by fairly low band width connections because all they need be capable of carrying is very small amounts of data and in this case fiche identification information.

By using such an arrangement, it is possible to have large users utilize their in place mainframe computers and the storage associated therewith as index computers 27.

Also shown in Figure 1 is the manner in which the system can be utilized in connection with remote image display terminals 19 of the same type as utilized in connection with the local area network. However, in this case, they are connected by a standard communications link 31 to the index computer 27 or to the local area network 17 by another standard communications link which are accessed in the similar manner as an index computer 27 or for its original application.

Thus it can be seen that data links of various types as for example via satellite and the like can be utilized for interconnecting the system to remote image display terminals.

From the foregoing it can be seen that the system shown in Figure 1 has great capacity for diversification in that it permits the use of local and remote image display terminals while still making it possible to interconnect with large systems.

A document digitizer 41 has been provided as a part of the system and can be utilized for digitizing specific documents by scanning the document electronically to convert a document to a binary bit stream which can be routed to remote locations for terminal display and hard copying. The document digitizer thus enables a document to be entered immediately into the system before being microfilmed and being placed on roll film.

In connection with all of the components of the system shown in Figure 1, it can be seen that all of them are in fact on-line. In fact, all the documents stored are on-line. The on-line connections for all the units of the system are made possible because a carrier sensed multiple access collision detect (CSMA/CD) protocol is utilized. This technique for this protocol is well known to those skilled in the art. With this technique, each device has the capability of asertaining when a communication link is free so that it can perform its functions. If a collision occurs the functions are stopped and started again with respect to the information which was being transmitted or being received.

Alternatively, an image display terminal 19 can be connected via coaxial cable to a rf modem of a microwave data link 36 to another rf modem connected via coxial cable to a LAN.

The system controller 11 comprises computer hardware and software and peripheral device interfaces to control all of the operations of the system as shown in Figure 1. The system controller also supervises the operation of the image disc storage units 12 whose function in the system is to receive document images in binary format from the image storage unit 16, to hold them in temporary or buffer storage mode and, upon command, to route them to image display terminals 19. The system controller is comprised of a Motorola (RTM) 68000 family based central proceesor unit (CPU). It also includes a 26 slot Intel (RTM) compatible Multibus card cage. It also includes a Fujitsu M2284 169 megabyte Winchester SMD disc drive and a cipher P880 magnetic tape drive and associated controllers.

In the present invention, the Multibus card cage (not shown) is of a conventional type and as shown schematically in Figure 2 has disposed therein on the back plane thereof, a main or host bus printed circuit (PC) board 51. The board 51 is provided with first and second sets of busses 52 and 53 extending in one direction on the board 51 and which in a Multibus are identified as P1 and P2. Typically the P1 bus is comprised of signal wires whereas the P2 bus typically contains wires or connectors which are not bused from one section to the other.

The first set of busses 52, also known as the P1 bus, is separated or interrupted electrically by cutting the bus wires into first, second and third sections 52a, 52b and 52c. The second set of busses 53, also known as P2 are separated electrically into first, second, third and fourth sections 53a, 53b, 53c, and 53d. It should be appreciated that the busses 52 and 53 can be electrically separated to provide additional sections.

Means is provided for mounting the host PC boards 56, the DMA ISU controller boards 68 and 69 and the memory boards 73 on the main bus PC board 51 at an angle thereto as, for example, 90° and to make electrical connections between the P1 and P2 terminals on the PC boards and the P1 and P2 busses on the main PC board and consists of connectors (not shown) mounted on the main board and connected to the P1 and P2 busses. The PC boards are carried in slots in the card cage (not shown) and have their P1 and P2 terminals fitted into the connectors (not shown) carried by the main board. By way of example, the main board 51 has connectors (not shown) that mate to the P1 (86 pin) board edge connector and has connectors (not shown) which mate to the P2 (60 pin) termi-

nals or board edge connector. Thus as shown, the host boards 56 and the DMA ISU boards 68 and 69 have their first sets of terminals P1 connected to the first section 52a of the first set of busses, the P1 bus on the pC board 51. The host boards 61 have their second set of terminals P2 connected to the first section 53a of the P2 bus on main board 51. The DMA ISU boards 68 and 69 have their second set of terminals P2 connected to the second and third sections of the P2 bus on the main board 51. The first and second sets, 71 and 72, of the memory boards 73 have their first terminal P1 connected to the second and third sections 52b and 52c of the first set of busses, the P1 bus and have their second set of terminals P2 connected to the fourth and fifth sections of the second set of busses, the P2 bus.

A plurality of host printed circuit boards 56 are provided to mate with the main or host PC board 51. The host PC boards 56 include reading from left to right in Figure 2, a CPU board 61, a memory board 62, a disc controller board 63, a tape controller board 64 and a local area network (LAN) controller board 66. Two direct memory access (DMA) image storage unit (ISU) controller boards 68 and 69 are provided. In addition two sets 71 and 72 of memory PC boards 73 are also provided. All of the PC boards are generally rectangular in configuration and each is provided with two sets of terminals along one edge identified as P1 and P2 which are adapted to be connected to the P1 and P2 busses 52 and 53. These two sets of terminals are often called edge card connectors having spaced apart fingers.

The P1 bus of the main board 51 is interrupted after the DMA ISU controller board 69 and is terminated via terminating resistors as per the Multibus specification. The second and third sections 53b and 53c of the P2 bus are connected by suitable wire connections represented schematically by flexible ribbon or tape cables 77 and 78 to the second and third sections of the 52b and 52c respectively P1 bus on the main board 51 of the memory PC boards 73. The other ends of the P1 bus sections 52b and 52c are then terminated via terminating resistors 81 and 82 respectively.

The sets 71 and 72 of memory cards each have the capability of accepting 16 megabytes of memory. The DMA ISU controller cards 68 and 69 function to act as a bridge between the host side of the P1 bus section 52a and the local P1 busses sections 52b and 52c and allows the host to access the memory on the local busses either by writing into the memory or reading back from the memory in the same manner as if the memory were actually resident on the host bus. The ISU controller cards 68 and 69 are also utilized for transferring data from the image storage unit into the local memory. The DMA ISU controller cards are capable of accessing the entire 16 megabytes of local memory and can place an image from the ISU anywhere in the local memory. The DMA ISU controller card also contains circuitry which permits it to interrupt the host to tell it that the transfer is complete and also contains registers which are written into by the host which tell the DMA ISU card where to place the data, when to start the transfer and similar functions.

The DMA ISU controller boards also include address extension registers which make it possible to obtain access to a memory far in excess of the addressing capabilities of the host CPU board. The address extension register permits the DMA ISU controller 68, 69 to appear to the host to occupy only 256k words of Multibus memory space while actually allowing access to an entire 8M words of storage per board for a total of 16 million words of "hidden" storage in the system. The address extension register makes it possible to specify the upper five bytes of the hidden address bus thereby creating 32 separate "pages" of 256K word memory segments per DMA ISU controller board. Since there are two such boards namely, 68 and 69, in the system and both residing in the same host memory space, this creates the 16M words of memory space.

The address extension register can be utilized to select one group of memory addresses which are going to be of interest in subsequent operations. When that series of operations has been completed, the next group of addresses are addressed in a similar type of operation as follows. This permits a CPU board that only has the capability to access, for example, one megabyte of memory to have complete access to the complete 16 megabytes capabilities of the local memories through the DMA ISU controller boards 68 and 69. From the foregoing it can be seen that a system has been provided which can be fabricated from standard Multibus components with relatively minor modifications to provide substantial local memory capabilities. With the system it is possible to utilize a large number of ISUs with the capability of having more than one ISU transferring data into a memory at one time because adequate bus band width has been provided. The system is capable of moving the information into the memory sufficiently fast to keep up with the ISU. In addition, the Multibus is available so that other operations can be performed on the Multibus even though information is being transferred into a memory from an ISU.

The DMA ISU controller boards 68 and 69, by having the additional addressing capability, translates addresses from the original Multibus to the extended memory Multibus provided by the local P1 bus memory 52b and 52c. The Multibus itself has a 16 megabyte addressing limitation, i.e., it only has 24 wires or 24 bits per address which addresses 16 megabytes.

Operation of the circuitry shown in Figure 2 can now be briefly described as follows. Let it be assumed that there is entered into the host cards 61, a request either to write into or to read out of one of the local memories provided by the sets 71 and 72 of memory cards 73. This signal is intercepted by one of the DMA ISU controller cards 68 and 69. The controller card then looks to see if there is a video input from the ISU occurring at the time and then time multiplexes it between the Multibus request and the ISU request. There is a block of logic circuitry on the DMA ISU controller cards which performs this function of controlling whether the host obtains access to the local memory bus or the video signal from the ISU obtains access to the local memory bus.

DMA ISU controller cards are address controllers which send addresses to the local memories incrementing them after each word from the ISU is written into the memory. Switching means is included which permits up to five different ISUs to share the same circuitry on the card. It also contains the capability for converting data which comes from the ISU in serial form into parallel form to store it 16 bits wide onto the local memory bus.

The system makes it possible to move high memory content traffic through the ISU into the system controller and into the local memory without tying up the Multibus. In addition, it makes it possible to provide much greater memory than normally would be the case. In other words, the extended memory bus gives more addressability than was accomplished by utilizing conventional Multibus addressing. Even though data is being moved into a memory, the Multibus itself is not tied up and is capable of performing Multibus transactions simultaneous with the data being moved into memory. In addition, there is given the ability to place a larger amount of memory on the system then would be the case if everything had to be mounted on one Multibus.

CLAIMS

1. In an electronic document image storage and retrieval system, at least one image storage unit, a plurality of image display terminals, each image display terminal having a screen and a keyboard, each image display unit being adapted to be coupled to the image storage unit, and a system controller coupled to the image storage unit for controlling the operation of the image storage unit, whereby information carried in the image storage unit can be supplied to an image display terminal upon receipt of a request from the image display terminal, the system controller including a main printed circuit board, said main printed circuit boards having first and second generally parallel sets of busses extending in one direction on said main printed circuit board, said first set of busses being separated electrically into first and second bus sections, said second set of busses being electrically separated into at least first, second and third bus sections, a plurality of host printed circuit boards and at least one direct memory access image storage unit controller printed circuit board and means for mounting said host printed circuit boards and said at least one direct memory access image storage unit controller printed circuit board on said main printed circuit board so that they extend at an angle therefrom and are electrically connected to the first section of the first set of busses and so that the host printed circuit boards are electrically connected to the first section of the second set of busses and the direct memory access image storage unit controller board is connected to the second section of the second set of busses, a plurality of memory printed circuit boards, means mounting said memory printed circuit boards on said main printed circuit boards so that they extend at an angle therefrom and are electrically connected to the second portion of the first set of busses and means for electrically connecting the second section of the second set of busses connected to the direct memory access image storage unit controller printed circuit board to the second section of the first set of busses.

2. A system as in Claim 1 wherein the first set of busses is divided into at least three electrically separated sections and the second set of busses is divided into at least four electrically separated sections, together with an additional direct memory access image storage unit controller printed circuit board and means for electrically connecting the additional direct memory access image storage unit controller printed circuit board to the first section of the first set of busses and to the third section of the second set of busses, a plurality of additional memory printed circuit boards, means mounting said plurality of additional circuit boards on said third section of said first set of busses and means interconnecting the busses of the third section of the second set of busses to the third section of the first set of busses.

3. A system as in Claim 1 wherein each direct memory access image storage unit controller printed circuit board has an address extension register.

4. A system as in Claim 1 together with an index computer coupled to the system controller.

5. A system according to Claim 1 and substantially as described herein.

6. An electronic document image storing and retrieval system substantially as described with reference to the accompanying drawings.

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